IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application of:	In-Duk SONG		
Application No.:	10/669,371	Confirmation No.:	3363
Filed:	September 25, 2003	Art Unit:	2871
For:	LIQUID CRYSTAL DISPLAY PANEL OF LINE-ON GLASS TYPE AND METHOD OF FABRICATING THE SAME	Examiner:	Lauren Nguyen

REQUEST FOR A PRE-APPEAL BRIEF CONFERENCE

MS AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant respectfully requests a Pre-Appeal Brief Conference with respect to the rejection of claims 1, 5, 6, 12-16 and 19-23, dated August 30, 2011. This request sets forth the independent claims under rejection and provides the below comments which address independent claim features and reasons (in bold below) why the last Office Action fails to make out a *prima facie* case of obviousness of those independent claims.

Claim 1 recites: A line-on glass liquid crystal display panel having sides and corners defined at intersections of the sides, comprising: a picture display part having liquid crystal cells at each intersection of first ~ (n)th gate lines and first ~ (m)th data lines; first~(m)th data pads extended from the first ~ (m)th data lines in an outer area of the picture display part; first~(n)th gate pads extended from the first ~ (n)th gate lines in the outer area of the picture display part;

a plurality of first line-on glass signal pads formed just beside the first data pad and a plurality of second line-on glass signal pads formed just beside the first gate pad, the first and second line-on glass signals pads are on respective intersecting sides which define one corner of

the outer area of the picture display part; **Kawaguchi discloses either using a TCP design or a COG design, but does not show any data pads on the outer portion of the lower LCD glass substrate. Kawaguchi has two prior art COG embodiments, i.e., Figs. 6 and 7. As stated above, no data pads are shown on the outer portion of the lower LCD glass substrate. Kawaguchi focuses on electrically interconnecting interconnection lines of adjacent tape carrier packages such that those interconnection lines and an opposite voltage use line can be prevented from crossing each other, and has no concept of providing these claimed signal pad features;**

a plurality of line-on glass type signal lines connecting the first and second line-on glass signal pads in the corner of the outer area of the picture display part for applying gate power voltage signals and gate control signals to gate drive ICs in order to drive gate signal lines of the picture display part;

a plurality of first dummy pads between the first line-on glass type signal pads and a plurality of second dummy pads between the second line-on glass type signal pads; **Kawaguchi completely fails to disclose this feature;** and

a plurality of dummy lines connecting the first and second dummy pads in the one corner of the outer area of the picture display part, wherein the plurality of first and second dummy lines are formed between the line-on glass type signal lines for applying a common voltage as a reference voltage to drive the liquid crystal cells with at least one layer of insulating film therebetween, wherein the insulating film covers the plurality of line-on glass type signal lines and the dummy lines are formed on the layer of insulating film. **Kawaguchi merely discloses opposite voltage use lines 11 (in Fig. 1A) in the LCD panel (10) itself rather than in a corner of the outer area of the picture display part, and discloses (in Fig. 2) opposite voltage use lines 22, as part of connection line 34 directly from a circuit board, without any pads on a corner of the outer area of the picture area. Moreover Kawaguchi only employs a single opposite-electrode use line 12 per TCP 24, and cannot meet the requirement of a plurality of dummy lines formed between the plurality of signal lines. Rather, Kawaguchi only forms a single opposite voltage line 12 adjacent to a plurality of signal lines 11. Additionally, Kawaguchi does not disclose the claimed insulating film feature.**

Yuda's relied-upon Fig. 10 embodiment uses a separate (from the LCD lower substrate) connection board 36 to connect its input signal lines 2a, and there is no explicit,

or inherent, (not just possible, and not just probable) disclosure of the claimed line on glass dummy pads. Presumably, any pads would be on the separate connection board, and not on the LCD lower substrate periphery.

Kim does not teach using a counter electrode line in between signal lines to reduce EMI. Kim merely discloses using a ground wire 700 between signal lines to reduce EMI.

So, no matter how these three references are combined, they cannot render obvious the claimed invention.

Claim 12 recites: A fabricating method of a line-on glass liquid crystal display panel having sides and corners defined at intersections of the sides, comprising:

forming first~ (n)th gate lines in a picture display part and a plurality of line-on glass signal lines in one corner of an outer area of the picture display part on a substrate for applying gate power voltage signals and gate control signals to gate drive ICs in order to drive gate signal lines of the picture display part;

forming at least one layer of insulating film to cover the line-on glass type signal lines;

forming first~(m)th data lines to cross the first~ (n)th gate lines in a picture display part and a dummy line that is located between the line-on glass signal lines on the insulating film for applying a common voltage as a reference voltage; and

forming first~(m)th data pads extended from the first~(m)th data lines on one side and first~ (n)th gate pads extended from the first~ (n)th gate lines on an intersecting side of the outer of the picture display part and forming first and second line-on glass signal pads just beside the first data pad and first gate pad, respectively and first dummy pads between the first line-on glass signal pads and second dummy pads between the second line-on glass pads, respectively, the intersecting sides defining one corner of the outer area of the picture display part,

wherein each of the plurality of the line-on glass signal lines is connected between the first and the second line-on glass signal pads in the one corner of the outer area of the picture display part.

The commonly recited structural features (common with respect to claim 1) that are formed by the claimed method steps are clearly not disclosed by the three applied references, either alone or in combination, for reasons presented above regarding claim 1 and, because of this, neither are the claimed method steps which form those features.

Claim 19 recites: A line-on glass liquid crystal display panel having sides and corners defined at intersections of the sides, comprising: a picture display part with a matrix of liquid crystal cells having a plurality of gate lines and date lines to cross each other; a gate pad and a data pad to drive the gate lines and data lines, respectively, the gate pad and the data pad are formed in an outer area of the picture display part of a low substrate; a plurality of line-on glass type signal lines located in one corner of the outer area of the picture display part of the lower substrate for applying drive signals to drive the liquid crystal cells, wherein the one corner of the outer area of the picture display part is defined by the intersection of two sides of said outer area of the lower substrate and wherein the gate pad is adjacent to one of the sides and the data pad is adjacent to the intersecting side;

a gate insulating layer covering the line-on glass type signal lines; **this feature is completely missing from the disclosures of Kawaguchi and Yuda; and**

a plurality of common voltage signal lines for applying a common voltage signal and being formed between line-on glass type signal lines, on the gate insulating layer; **this feature is also completely missing from Kawaguchi and Yuda. Kawaguchi's single opposite voltage use line 12 is simply placed adjacent to the plurality of signal lines 11, and not between them, and these is no disclosure of line 12 being on a gate insulating layer. Yuda has no disclosure of its input signal lines being on a gate insulation layer, either;**

wherein at least one of the plurality of common voltage lines applies the common voltage signal through a silver (Ag) dot to a common electrode that is formed on an entire surface of an upper substrate. **Neither Kawaguchi not Yuda discloses that its opposite voltage electrode is formed on the entire surface of the upper substrate.**

Claim 21 recites: A line-on glass liquid crystal display panel having sides and corners defined at intersections of the sides, comprising: a picture display part with a matrix of liquid crystal cells having a plurality of gate lines and data lines to cross each other; a gate pad and a data pad to drive the gate lines and data lines, respectively, the gate pad and the data pad are formed in an outer area of the picture display part of a low substrate on respective intersecting sides which define one corner; a plurality of line-on glass type signal lines located in one corner of the outer area of the picture display part of the lower substrate extending from one side to the other intersecting side that defines the one corner for applying drive gate signals to drive the

liquid crystal cells, wherein the plurality of line-on-glass signal lines are located between the gate pad and the data pad; and

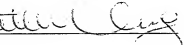
a common voltage line located in the one corner, wherein the common voltage line is adjacent to both the gate pad and the data pad. **Neither Kawaguchi nor Yuda shows this feature. Neither of Kawaguchi's common voltage lines 12 and 22 is disclosed as being located in one corner of the outer area of the picture display part of the lower substrate, either explicitly or inherently. Nor does Yuda disclose that its input signal lines 2a contain a common voltage line at all, let alone, as claimed, i.e., as being adjacent to both a gate pad and a data pad, both of which are located in an outer area of the picture display part of a lower substrate on respective intersecting sides which define one corner. In fact, Yuda does not teach that its gate pad and data pad are located, as claimed. Moreover, there is no explicit or inherent (necessary) disclosure that Yuda's gate pads and data pads are located on the outer area of the picture display part of the substrate. Moreover, because a special connection board is provided, those pads would be expected to be located on element 36.**

For the foregoing reasons, Applicant respectfully submits that the Office Action fails to make out a *prima facie* case of obviousness of the claimed invention, and respectfully requests that the rejection of claims 1, 5, 6, 12-16 and 18 be withdrawn and this Application be passed to issue.

If necessary, the Director is hereby authorized in this, concurrent, and future replies to charge any fees required during the pendency of the above-identified application or credit any overpayment to Deposit Account No. 02-2448.

Dated: December 9, 2011

Respectfully submitted,

By 

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